PCI Express SFF-8639 Module

Specification

Revision 4.0, Version 0.3

September 18, 2018

Note to Reviewers:

This 0.3 draft specification includes only the high level changes for the PCI Express Gen 4.0 SFF-8639 Module specification as approved by the SFF-Connector workgroup. Please provide feedback on these items and any additional requirements that you believe should be covered in the Gen 4.0 SFF-8639 Module specification.

1) Support existing architectural models
   - Connected directly from system board to SFF-8639 module
   - Cabled directly from system board to SFF-8639 module
   - Cabled from system board to backplane to SFF-8639 module

2) Add new data transfer rate of 16 GT/s NRZ

3) Enable Separate REFCLK Independent SSC (SRIS) and Separate REFCLK No SSC (SRNS)

4) Remove the REFCLK Phase Jitter Specification and reference the applicable section of the base specification

5) Enable the use of re-timers
   - Prohibit use of re-timers on the SFF-8639 modules
   - Allocate a maximum of two re-timers to the SFF-8639 system

6) Add insertion loss requirement for SFF-8639 module (Connector footprint to die)

7) Extend electrical characteristic requirements (DDIL, DDRL, DDNEXT) for connector interface to 16 GT/s

8) Specify Transmitter Equalization for 16 GT/s transfer rate (Add transmitter preset settings)

9) Specify new Transmitter Eye Diagram Height and Width requirements for 16 GT/s

10) Specify Transmitter Path Pulse Width Jitter Specification (this is a new parameter which only applies to 16 GT/s)

11) Specify new Receiver Path Sensitivity Requirements for 16 GT/s